Amendments To The Claims:

This listing of the claims will replace all prior versions and listings of claims for this application:

Listing of Claims:

Claims 1-24 (Canceled).

25. (Currently amended) A semiconductor device package, comprising:

a semiconductor device having diced edges;

a dielectric substrate having diced edges;

a metal layer ~~formed between said semiconductor device and said dielectric substrate, said metal layer~~ having diced edges;

a ball grid array on said dielectric substrate, said dielectric substrate ~~and said metal layer~~ being located between said semiconductor device and said ball grid array; and

electrical connections between said semiconductor device and said ball grid array,

wherein said metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said metal layer edges, so as to provide said package with aligned edges.

26. (Original) The package of claim 25, wherein said metal layer provides a ground plane for said electrical connections.

Claim 27 (Canceled).

28. (Original) The package of claim 25, wherein said metal layer is arranged to dissipate heat from said semiconductor device.

29. (Original) The package of claim 25, wherein said metal layer comprises copper.

30. (Previously presented) The package of claim 25, wherein said connections comprise wire bonds.

31. (Original) The package of claim 25, wherein said connections comprise conductive vias.

32. (Original) The package of claim 31, wherein said connections further comprise conductive traces on opposite sides of said substrate.

33. (Original) The package of claim 32, further comprising solder bumps on said semiconductor device, said bumps being connected to said traces.

34. (Previously presented) The package of claim 25, further comprising an insulative solder mask for covering said dielectric substrate.

Claims 35-38 (Canceled).

39. (Previously presented) The package of claim 25, wherein the metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

40. (Previously presented) A semiconductor device package, comprising:

a semiconductor device having diced edges;

a dielectric substrate having diced edges over an upper side of said semiconductor device;

a first metal layer having diced edges below a lower side of said semiconductor device;

a ball grid array over said dielectric substrate and on an opposite side of said dielectric substrate than said semiconductor device; and

electrical connections between said semiconductor device and said ball grid array.

41. (Previously presented) The semiconductor package of claim 40, wherein said first metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said first metal layer edges, so as to provide said package with aligned edges.

42. (Previously presented) The semiconductor package of claim 40, wherein said first metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

43. (Previously presented) The semiconductor package of claim 40, further comprising a second metal layer below a lower side of said first metal layer and on an opposite side of said first metal layer from said semiconductor device.

44. (Previously presented) The semiconductor package of claim 43, wherein said first metal layer has a thickness of about 0.00254 millimeters.

45. (Previously presented) The semiconductor package of claim 43, wherein said second metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

46. (Previously presented) The semiconductor package of claim 43, wherein the second metal layer has diced edges aligned with edges of said first metal layer, said semiconductor device edges, and said dielectric substrate edges.

47. (New) A semiconductor structure comprising:

a plurality of semiconductor chips formed on a wafer;

a plurality of ball grid arrays mounted on a dielectric substrate such that said plurality of ball grid arrays face away from said wafer, each ball grid array respectively associated with one of said plurality of semiconductor chips on said wafer;

electrical connections between each ball grid array and an associated semiconductor chip; and

a first metal layer attached to the semiconductor wafer, said metal layer having sufficient stiffness to enable simultaneous dicing of said wafer, said dielectric substrate, and said metal layer.

48. (New) The semiconductor structure of claim 47, wherein the dielectric substrate comprises a thin, flexible film.

49. (New) The semiconductor structure of claim 48, wherein the dielectric substrate comprises any one of FR-4BT resins, epoxy, polymide, KAPTON, UPLEX, and ceramic material.

50. (New) The semiconductor structure of claim 47, wherein the electrical connections comprise at least one of wire bonds, bond pads, circuit traces, and ball pads.

51. (New) The semiconductor structure of claim 47, further comprising a second metal layer surface connected to the first metal layer.

52. (New) A semiconductor device package, comprising:

a semiconductor device having at least one flip chip bump contact;

a dielectric substrate having a via, said via being filled with a conductive material;

a ball grid array mounted on said dielectric substrate, said dielectric substrate being located between said semiconductor device and said ball grid array; and

a metal layer having attached to the semiconductor device, said metal layer having sufficient stiffness to enable the simultaneous dicing of said dielectric substrate and said semiconductor device from a structure comprising a wafer and a dielectric substrate layer attached thereto.

53. (New) The semiconductor device package of claim 52, further comprising circuit traces on the surface of the dielectric substrate, for electrically connecting the ball grid array mounted on the dielectric substrate to the semiconductor device.

54. (New) The semiconductor device package of claim 53, wherein the circuit traces comprise at least an interior trace patterned on a top surface of the dielectric substrate and at least one exterior trace patterned on the bottom surface of the substrate.

55. (New) The semiconductor device package of claim 54, wherein at least one interior trace is in contract with at least one flip chip bump on the surface of the semiconductor device and said at least one exterior trace is connected to said at least one interior trace through the conductively filled via.

56. (New) The semiconductor device package of claim 52, wherein the conductively filled via has a diameter within the range of approximately 25 microns to approximately 200 microns.